N-Channel Enhancement Mode MOSFET

2N7002V

Features

HF

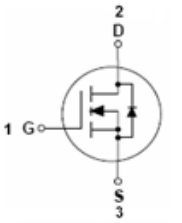
- Advanced trench cell design
- Extremely low threshold voltage

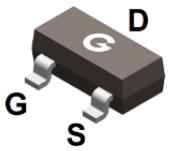
Typical Applications

- N-channel enhancement mode effect transistor

Mechanical Data

- Case: SOT-23
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte Tin-Plated Leads, Solderability-per MIL-STD-202, Method 208





SOT-23

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
2N7002V	SOT-23	3000 pcs / Tape & Reel	7002V

Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	V
Gate-to-Source Voltage	V_{GSS}	±30	V
Continuous Drain Current (T_C = 25°C) *1	I_D	300	mA
Continuous Drain Current (T_A = 25°C) *1	I_D	250	mA
Continuous Drain Current (T_A = 70°C) *1		200	mA
Pulsed Drain Current (t_p = 10μs, T_A = 25°C)	I_{DM}	2000	mA
Single Pulse Avalanche Energy *3	E_{AS}	0.11	mJ
Power Dissipation *1	P_D	0.35	W
Operating Junction Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case*1	$R_{\theta JC}$	-	217	230	°C/W
Thermal Resistance Junction-to-Air *1	$R_{\theta JA}$	-	319	357	°C/W

Electrical Characteristics (@ T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60V, V_{GS} = 0V	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±30V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$R_{DS(ON)}$	Drain-Source On-resistance *2	V_{GS} = 10V, I_D = 0.5A	-	0.9	3	Ω
		V_{GS} = 4.5V, I_D = 0.075A	-	1	3.5	
$V_{GS(TH)}$	Static Drain-Source On-resistance	V_{DS} = V_{GS}, I_D = 250μA	1	1.5	2.5	V
R_G	Gate Resistance	V_{GS} = 0V, f = 1MHz	-	51	-	Ω
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	-	35	-	pF
C_{OSS}	Output Capacitance		-	7	-	
C_{RSS}	Reverse Transfer Capacitance		-	3	-	
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time *4	V_{DD} = 30V V_{GS} = 10V R_G = 25Ω I_D = 0.2A	-	3.6	-	ns
t_r	Turn-on Rise Time *4		-	3.3	-	
$t_{d(off)}$	Turn-Off Delay Time *4		-	20	-	
t_f	Turn-Off Fall Time *4		-	11	-	
Q_G	Total Gate-Charge	V_{DD} = 10V V_{GS} = 4.5V I_D = 0.2A	-	0.41	-	nC
Q_{GS}	Gate to Source Charge		-	0.15	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	0.2	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage *2	I_S = 0.3A, V_{GS} = 0V	-	1.09	1.5	V

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%
3. The E_{AS} data shows Max. rating. The test condition is V_{DD} = 30V, V_{GS} = 15V, L = 0.1mH
4. Guaranteed by design, not subject to production

Ratings and Characteristic Curves (@ T_A = 25°C unless otherwise specified)

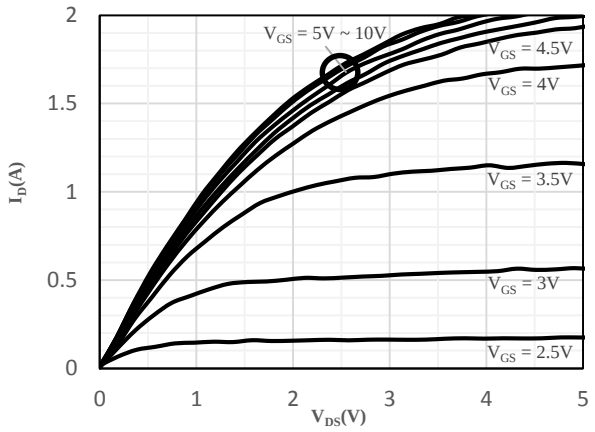


Fig 1 Typical Output Characteristics

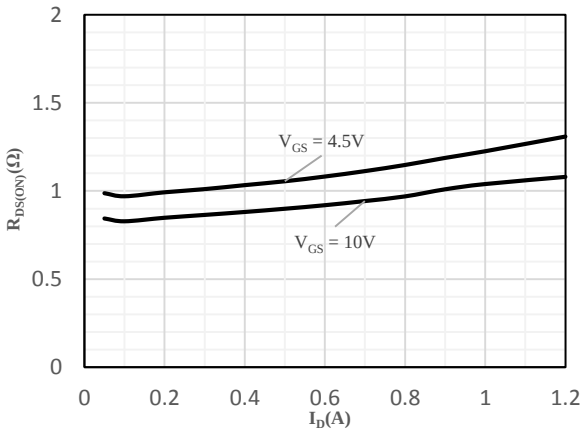


Fig 2 On-Resistance vs. Drain Current and Gate Voltage

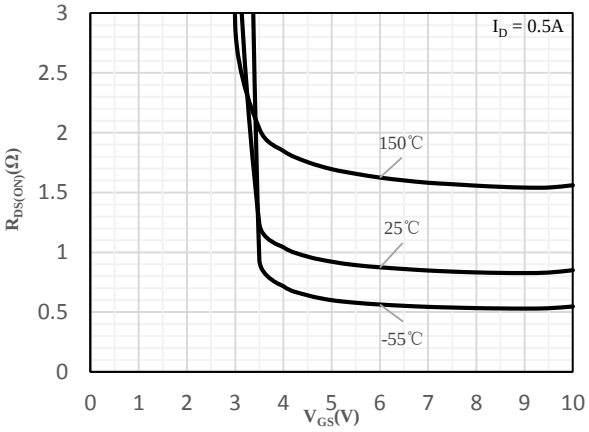


Fig 3 On-Resistance vs. Gate-Source Voltage

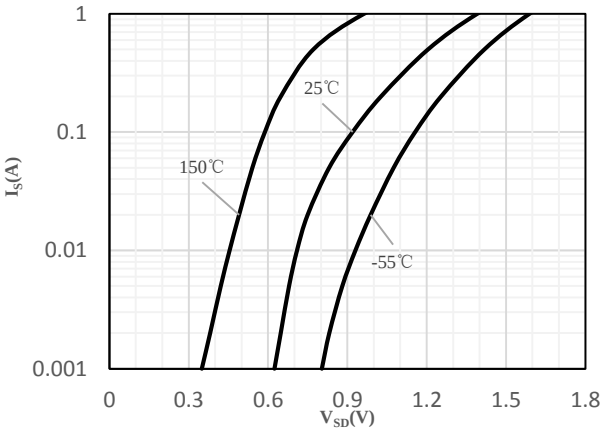


Fig 4 Body-Diode Characteristics

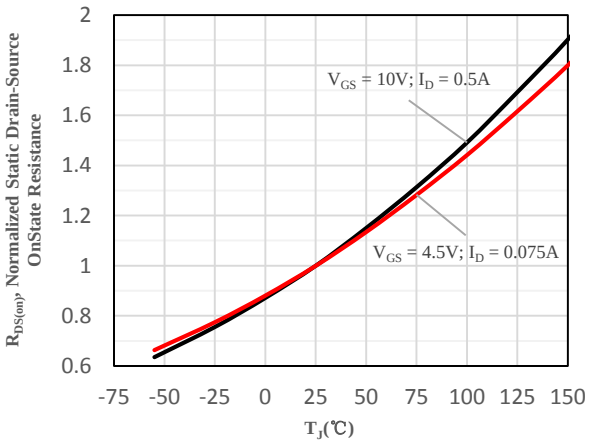


Fig 5 Normalized On-Resistance vs. Junction Temperature

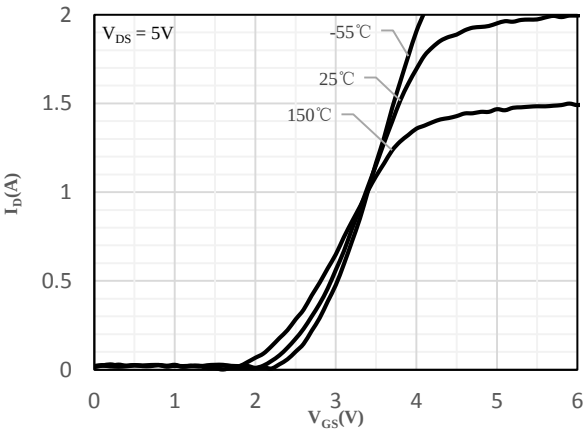


Fig 6 Transfer Characteristics

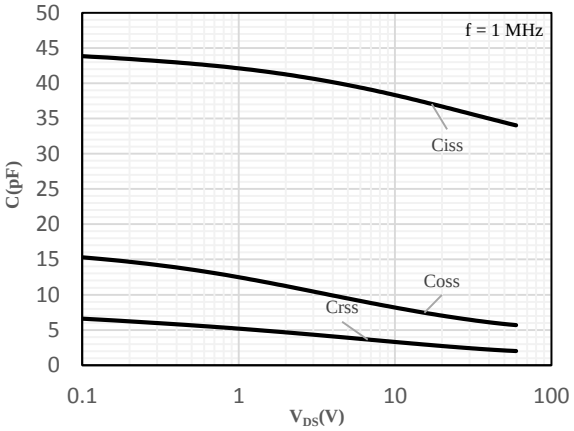


Fig 7 Capacitance Characteristics

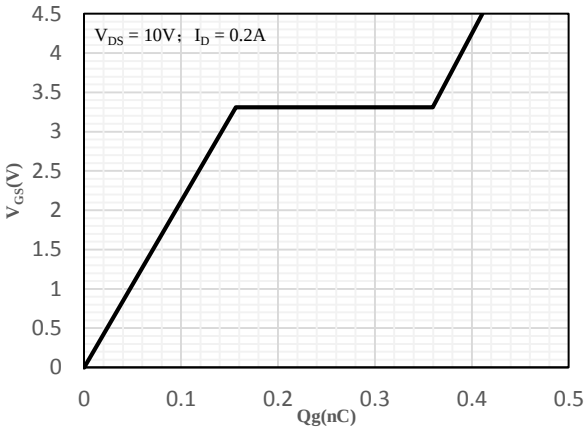


Fig 8 Gate-Charge Characteristics

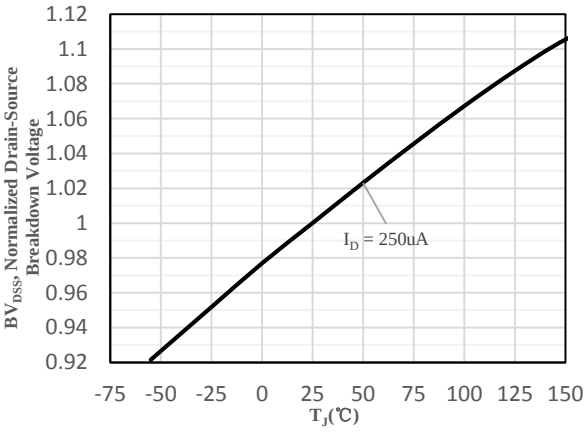


Fig 9 Normalized Breakdown Voltage vs. Junction Temperature

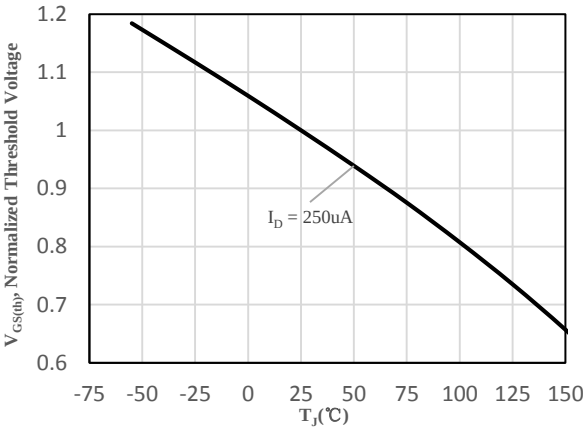


Fig 10 Normalized $V_{GS(th)}$ vs. Junction Temperature

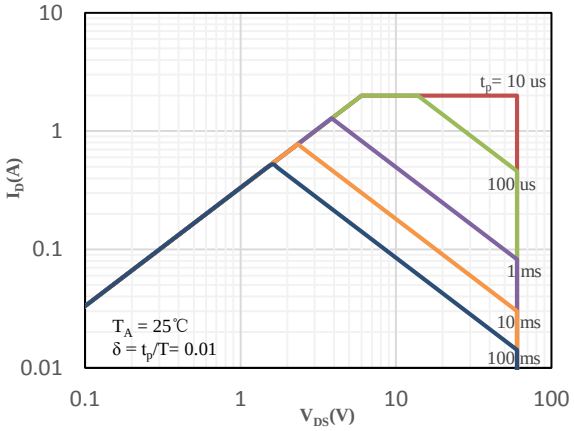


Fig 11 Safe Operation Area

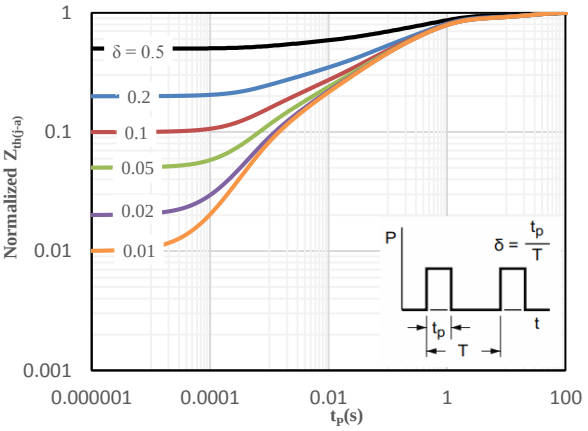
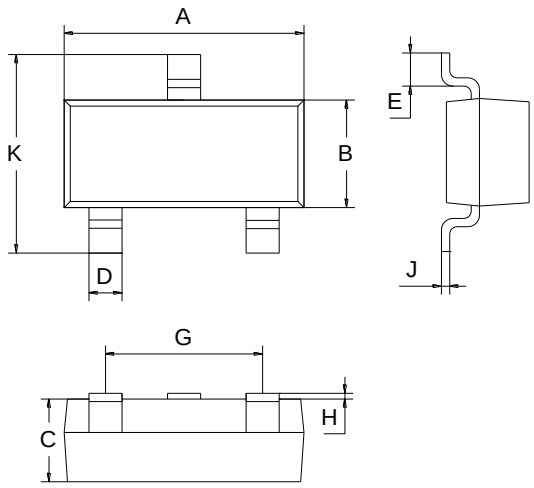


Fig 12 Normalized Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)

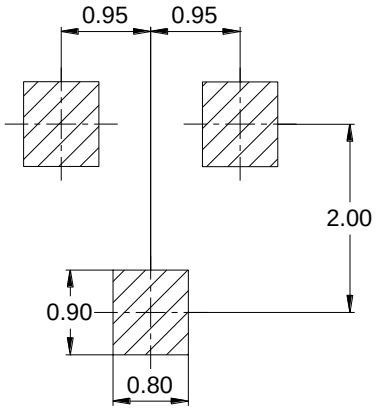
SOT-23



SOT-23		
Dimension	**Min.**	**Max.**
A	2.70	3.10
B	1.10	1.50
C	0.90	1.10
D	0.30	0.50
E	0.35	0.48
G	1.80	2.00
H	0.02	0.10
J	0.05	0.15
K	2.20	2.60

Mounting Pad Layout (Unit: mm)

SOT-23



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