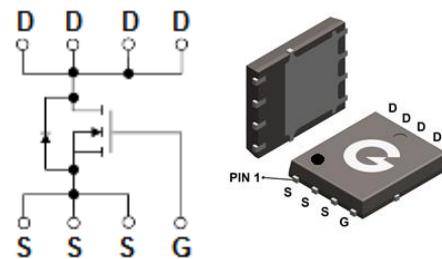


## Features

- Super low gate charge
- Green device available
- Excellent  $C_{dV}$  /  $dV/dI$  effect decline
- Advanced high cell density trench technology

**HF**



**PDFN5x6-8L**

## Mechanical Data

- Case: PDFN5x6-8L
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208

## Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
BL033N03-5DL8	PDFN5x6-8L	5000 pcs / Tape & Reel	033N03

## Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current ( $T_c = 25^\circ\text{C}$ ) <sup>*1</sup>	$I_D$	150	A
Continuous Drain Current ( $T_c = 100^\circ\text{C}$ ) <sup>*1</sup>		100	A
Pulsed Drain Current <sup>*2</sup>	$I_{DM}$	450	A

## Thermal Characteristics

Parameter	Symbol	Value	Unit
Power Dissipation ( $T_c = 25^\circ\text{C}$ ) <sup>*3</sup>	$P_D$	130	W
Thermal Resistance Junction-to-Air <sup>*1</sup>	$R_{\theta JA}$	25	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Case <sup>*1</sup>	$R_{\theta JC}$	2.8	$^\circ\text{C}/\text{W}$
Operating Junction Temperature Range	$T_J$	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

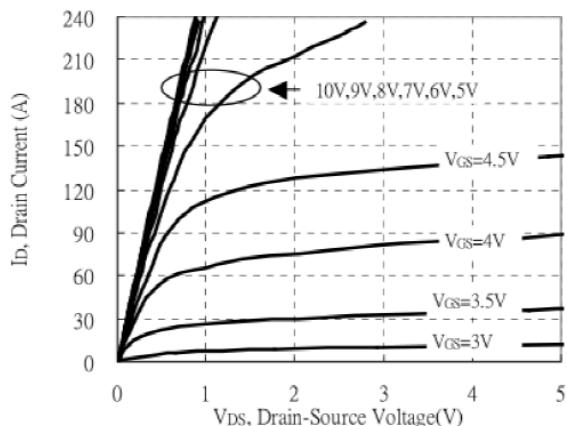
**Electrical Characteristics** (@  $T_A = 25^\circ\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
$V_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	30	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_C = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 24\text{V}, V_{GS} = 0\text{V}, T_C = 55^\circ\text{C}$	-	-	5	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$R_{DS(ON)}$	Static Drain-Source On-resistance <sup>*2</sup>	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	-	2.3	3.3	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$	-	4.0	6.3	$\text{m}\Omega$
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.2	-	2.5	V
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$	-	3580	-	pF
$C_{OSS}$	Output Capacitance		-	358	-	
$C_{RSS}$	Reverse Transfer Capacitance		-	305	-	
<b>Switching Characteristics</b>						
$t_{d(\text{ON})}$	Turn-on Delay Time	$V_{DD} = 20\text{V}$ $V_{GS} = 10\text{V}$ $R_G = 3.0\Omega$ $I_D = 20\text{A}$	-	13	-	ns
$t_r$	Turn-on Rise Time		-	115	-	
$t_{d(\text{OFF})}$	Turn-Off Delay Time		-	23	-	
$t_f$	Turn-Off Fall Time		-	58	-	
$Q_G$	Total Gate-Charge	$V_{DD} = 15\text{V}$ $V_{GS} = 10\text{V}$ $I_D = 20\text{A}$	-	63	-	nC
$Q_{GS}$	Gate to Source Charge		-	9	-	
$Q_{GD}$	Gate to Drain (Miller) Charge		-	13.5	-	
<b>Source-Drain Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sup>*2</sup>	$I_{SD} = 20\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	-	-	1.2	V
$I_s$	Diode Continuous Forward Current <sup>*1, 4</sup>		-	-	150	A
$I_{SM}$	Pulsed Source-Drain Current <sup>*2, 4</sup>		-	-	450	A
$t_{rr}$	Reverse Recovery Time	$T_J = 25^\circ\text{C}, I_F = 20\text{A},$ $di/dt=100\text{A}/\mu\text{s}$	-	54	-	nS
$Q_{rr}$	Reverse Recovery Charge		-	98	-	nC

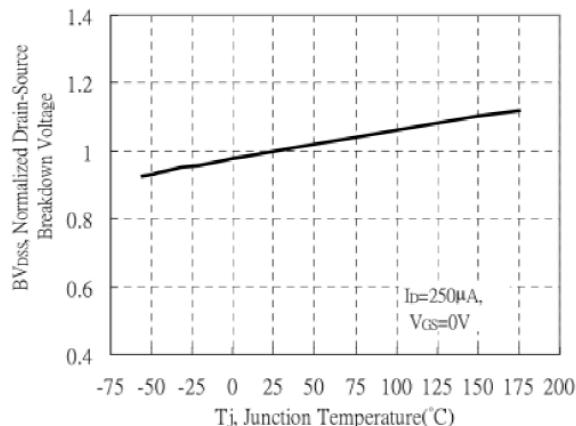
Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper
2. The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$
3. The power dissipation is limited by  $175^\circ\text{C}$  junction temperature
4. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation

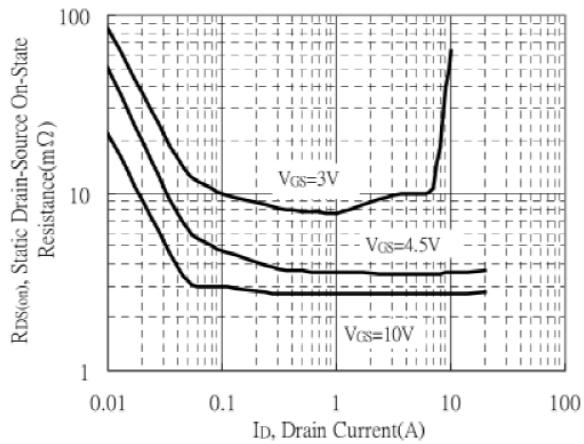
## Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)



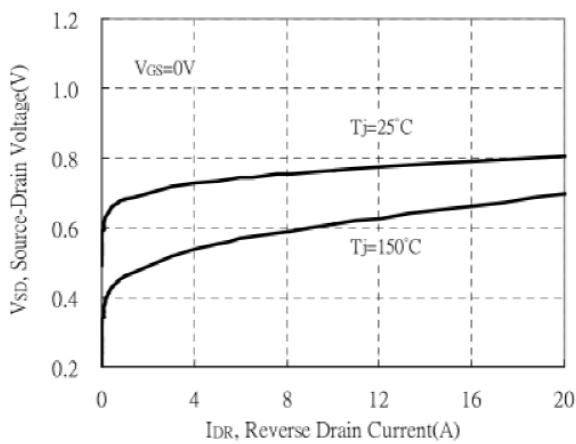
**Figure1: Typical Output Characteristics**



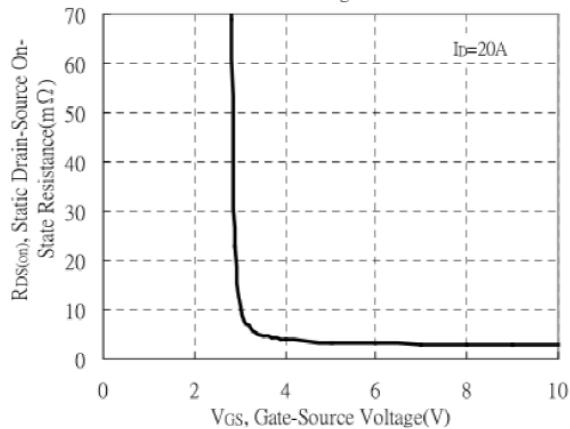
**Figure2: Breakdown Voltage vs Ambient Temperature**



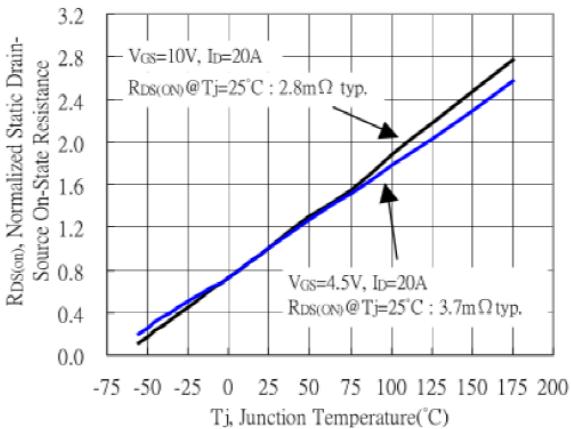
**Figure3: Static Drain-Source On-State resistance vs Drain Current**



**Figure4: Reverse Drain Current vs Source-Drain Voltage**



**Figure5: Static Drain-Source On-State Resistance vs Gate-Source Voltage**



**Figure6: Drain-Source On-State Resistance vs Junction Temperature**

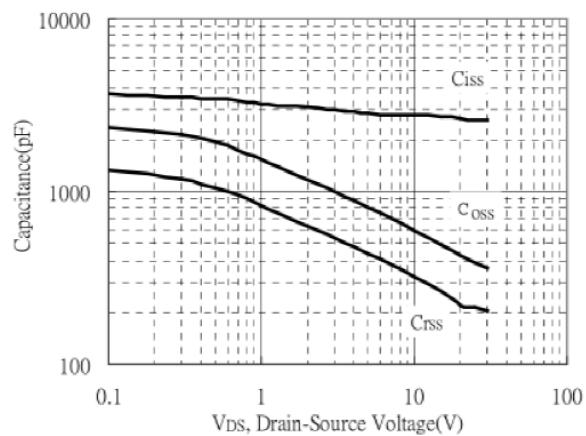


Figure7: Capacitance vs Drain-to-Source Voltage

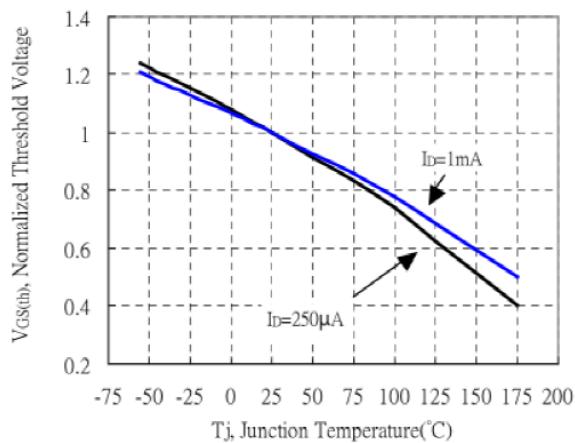


Figure8: Threshold Voltage vs Junction Temperarture

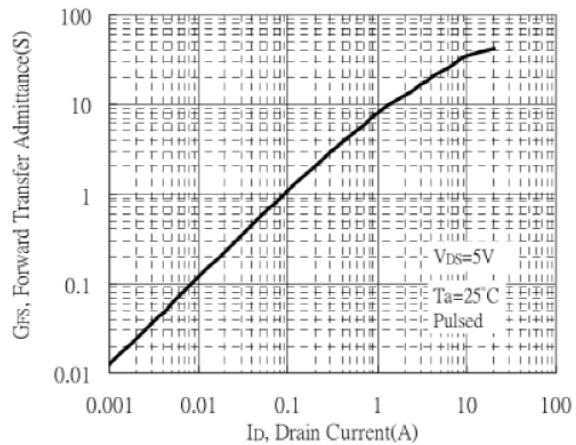


Figure9: Forward Transfer Admittance vs Drain Current

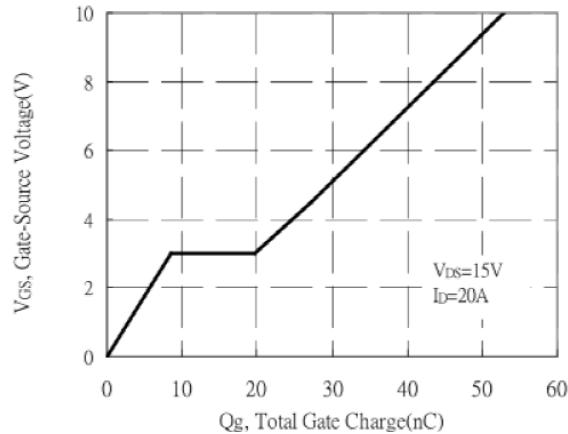


Figure10: Gate Charge Characteristics

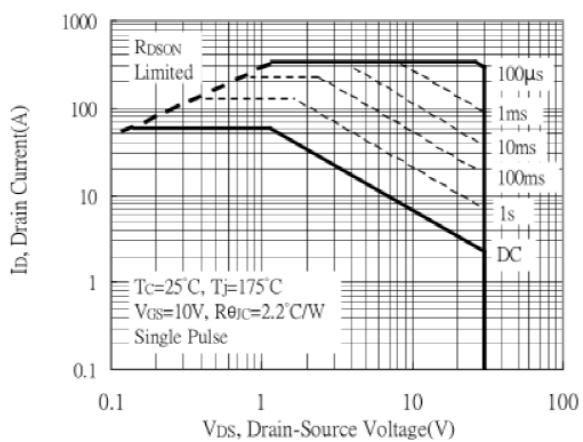


Figure11: Maximum Safe Operating Area

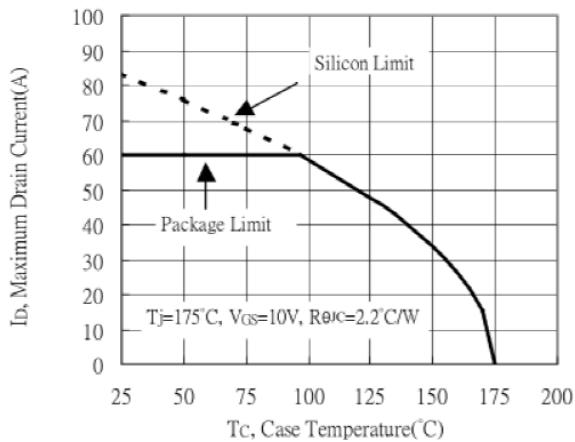
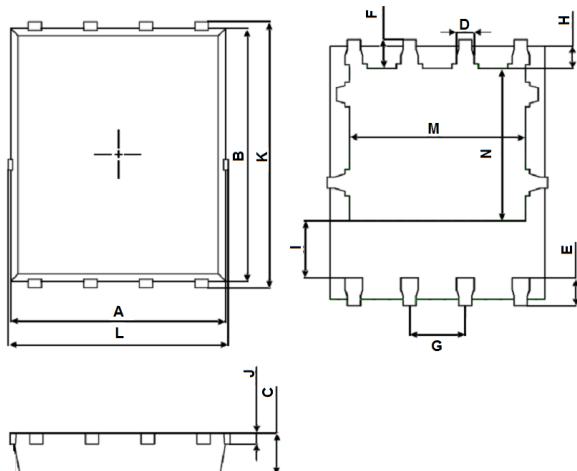
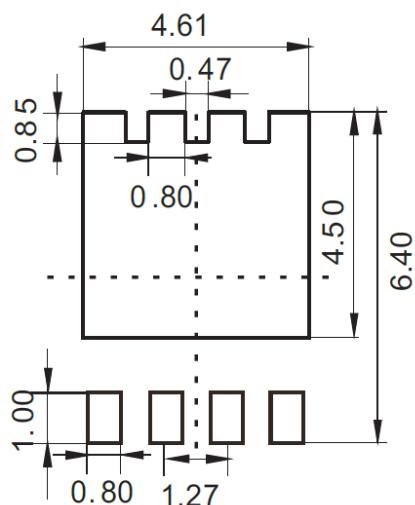


Figure12: Maximum Drain Current vs Case Temperature

**Package Outline Dimensions** (Unit: mm)


PDFN5x6-8L		
Dimension	Min.	Max.
A	4.824	4.976
B	5.674	5.826
C	0.900	1.000
D	0.350	0.450
E	0.559	0.711
F	0.574	0.726
G	1.250	1.290
H	0.424	0.576
I	1.190	1.390
J	0.154	0.354
K	5.974	6.126
L	4.944	5.096
M	3.910	4.110
N	3.375	3.575

**Mounting Pad Layout** (Unit: mm)

**PDFN5x6-8L**

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