

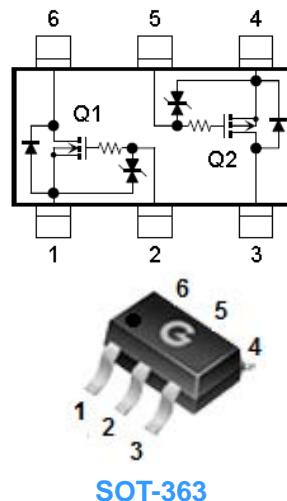
Features

- Extremely low threshold voltage
- ESD protected
- Advanced trench cell design

HF

Mechanical Data

- Case: SOT-363
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
BL1415DW	SOT-363	3000 pcs / Tape & Reel	K5

Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Q1	Q2	Unit
Drain-to-Source Voltage	V_{DSS}	30	-30	V
Gate-to-Source Voltage	V_{GSS}	± 10	± 10	V
Continuous Drain Current($V_{GS} = \pm 4.5\text{V}$) *1	I_D	0.78	-0.36	A
Pulsed Drain Current($V_{GS} = \pm 4.5\text{V}$) *1,2	I_{DM}	3.1	-1.4	A

Thermal Characteristics

Parameter	Symbol	Value	Unit
Power Dissipation($T_A = 25^\circ\text{C}$) *1	P_D	0.3	W
Thermal Resistance Junction-to-Air *1	$R_{\theta JA}$	416	$^\circ\text{C}/\text{W}$
Operating Junction Temperature Range	T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Electrical Characteristics-Q1 (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	30	-	-	V
$I_{DS(0)}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 10\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 10	μA
On Characteristics						
$R_{DS(ON)}$	Static Drain-Source On-resistance * ²	$V_{GS} = 4.5\text{V}$, $I_D = 0.5\text{A}$	-	-	1.2	Ω
		$V_{GS} = 2.5\text{V}$, $I_D = 0.2\text{A}$	-	-	1.6	Ω
		$V_{GS} = 1.8\text{V}$, $I_D = 0.1\text{A}$	-	-	2	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	0.5	-	1.0	V
Dynamic Characteristics * ³						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{V}$ $V_{DS} = 15\text{V}$ $f = 1.0\text{MHz}$	-	54	-	pF
C_{OSS}	Output Capacitance		-	9.4	-	
C_{RSS}	Reverse Transfer Capacitance		-	4.4	-	
Switching Characteristics * ³						
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD} = 15\text{V}$, $V_{GS} = 4.5\text{V}$ $R_G = 4.5\Omega$, $R_L = 30\Omega$ $I_D = 0.5\text{A}$	-	1.8	-	ns
t_r	Turn-on Rise Time		-	18	-	
$t_{d(OFF)}$	Turn-Off Delay Time		-	29	-	
t_f	Turn-Off Fall Time		-	22	-	
Q_G	Total Gate-Charge	$V_{DD} = 15\text{V}$ $V_{GS} = 4.5\text{V}$ $I_D = 0.5\text{A}$	-	0.8	-	nC
Q_{GS}	Gate to Source Charge		-	0.2	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	0.08	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage * ²	$I_{SD} = 0.5\text{A}$, $V_{GS} = 0\text{V}$	-	-	1.2	V

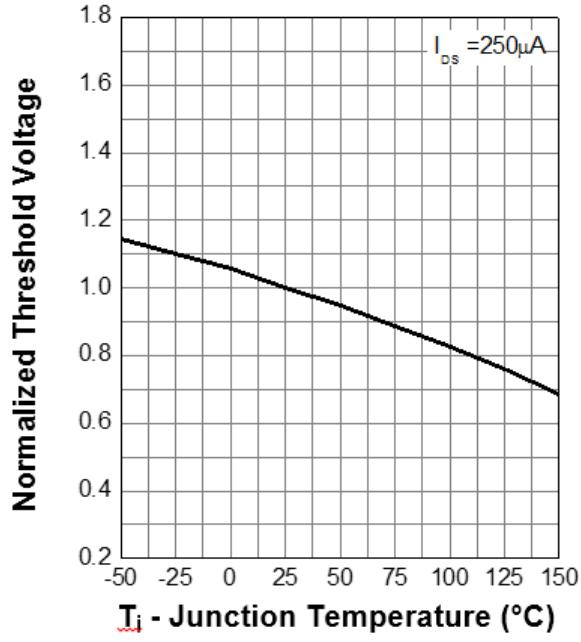
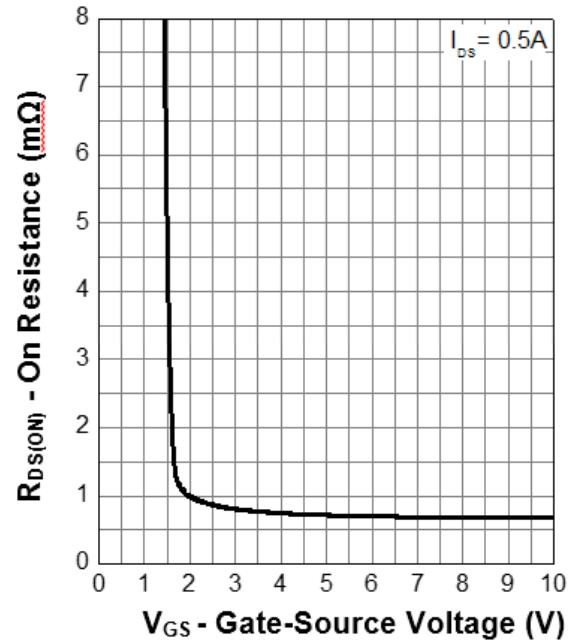
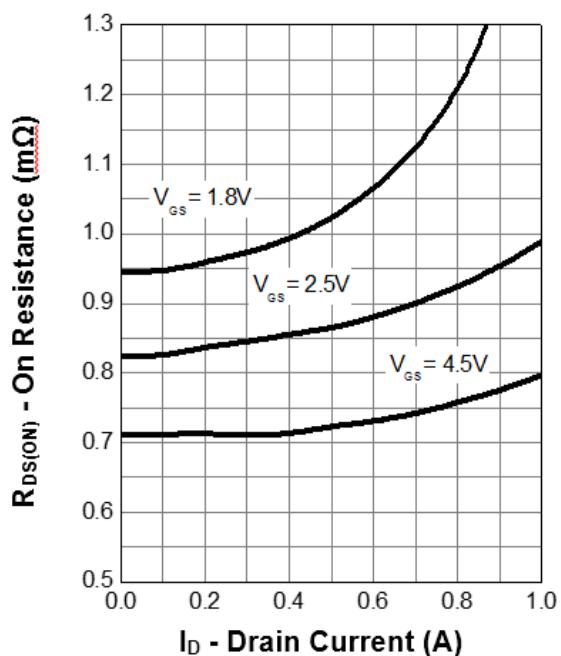
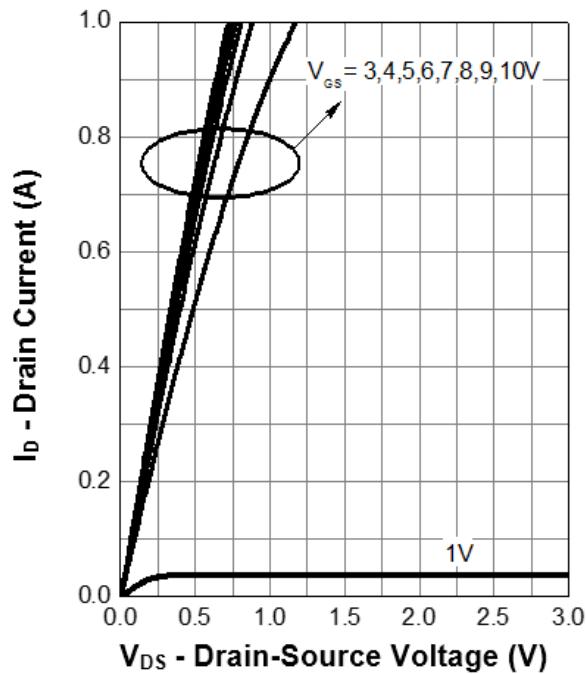
Electrical Characteristics-Q2 (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-30	-	-	V
$I_{DS(on)}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$	-	-	-1	μA
I_{GSS}	Gate-Body Leakage Current	$V_{GS} = \pm 8\text{V}, V_{DS} = 0\text{V}$	-	-	± 10	μA
On Characteristics						
$R_{DS(on)}$	Static Drain-Source On-resistance *2	$V_{GS} = -4.5\text{V}, I_D = -0.3\text{A}$	-	-	2.5	Ω
		$V_{GS} = -2.5\text{V}, I_D = -0.2\text{A}$	-	-	2.9	Ω
		$V_{GS} = -1.8\text{V}, I_D = -0.1\text{A}$	-	-	5	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.4	-	-1.0	V
Dynamic Characteristics *3						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{V}$ $V_{DS} = -10\text{V}$ $f = 1.0\text{MHz}$	-	50	-	pF
C_{OSS}	Output Capacitance		-	6	-	
C_{RSS}	Reverse Transfer Capacitance		-	5	-	
Switching Characteristics *3						
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD} = -10\text{V}, V_{GS} = -4.5\text{V}$ $R_G = 6\Omega, R_L = 150\Omega$ $I_D = -0.1\text{A}$	-	3.4	-	ns
t_r	Turn-on Rise Time		-	13	-	
$t_{d(OFF)}$	Turn-Off Delay Time		-	37	-	
t_f	Turn-Off Fall Time		-	23	-	
Q_G	Total Gate-Charge	$V_{DD} = -10\text{V}$ $V_{GS} = -4.5\text{V}$ $I_D = -0.1\text{A}$	-	1.22	-	nC
Q_{GS}	Gate to Source Charge		-	0.33	-	
Q_{GD}	Gate to Drain (Miller) Charge		-	0.22	-	
Source-Drain Diode Characteristics						
V_{SD}	Diode Forward Voltage *2	$I_{SD} = -0.3\text{ A}, V_{GS} = 0\text{V}$	-	-	-1.3	V

Notes:

1. Surface mounted on 1 in² pad area, $t \leq 10$ sec
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. Guaranteed by design, not subject to production testing

Ratings and Characteristics Curves-Q1 (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)



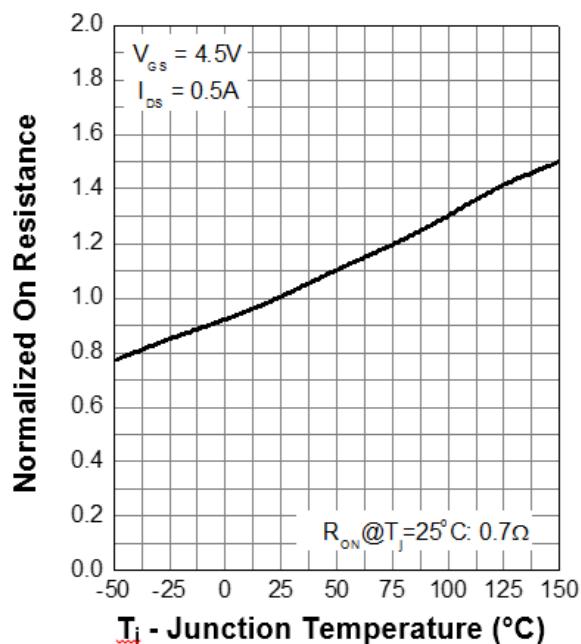


Fig. 5 On-Resistance vs. Junction Temperature

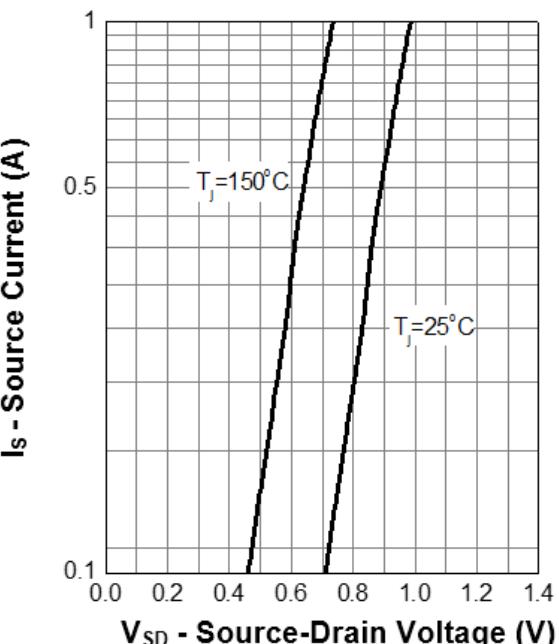


Fig. 6 Body-Diode Characteristics

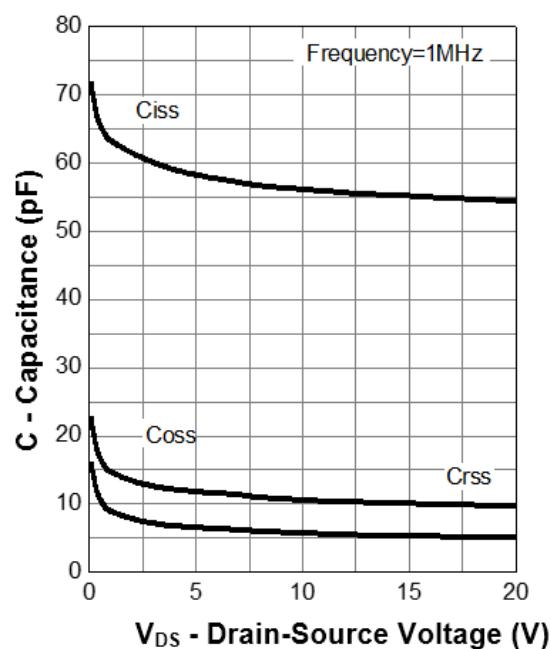


Fig. 7 Capacitance Characteristics

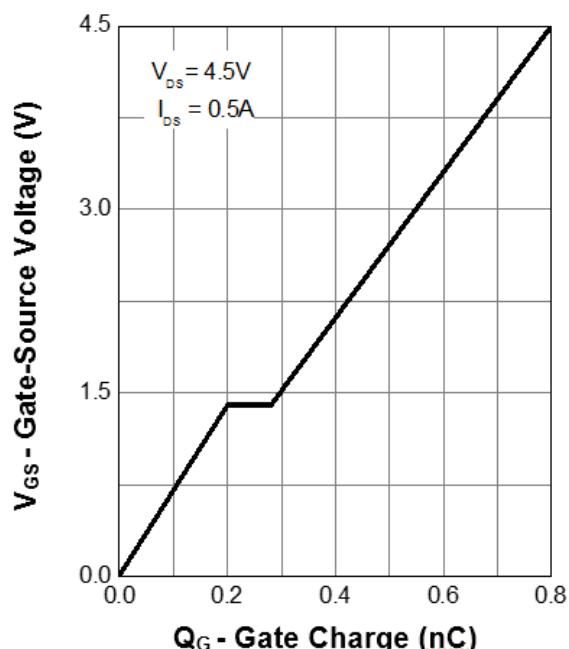


Fig. 8 Gate-Charge Characteristics

Ratings and Characteristics Curves-Q2 (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

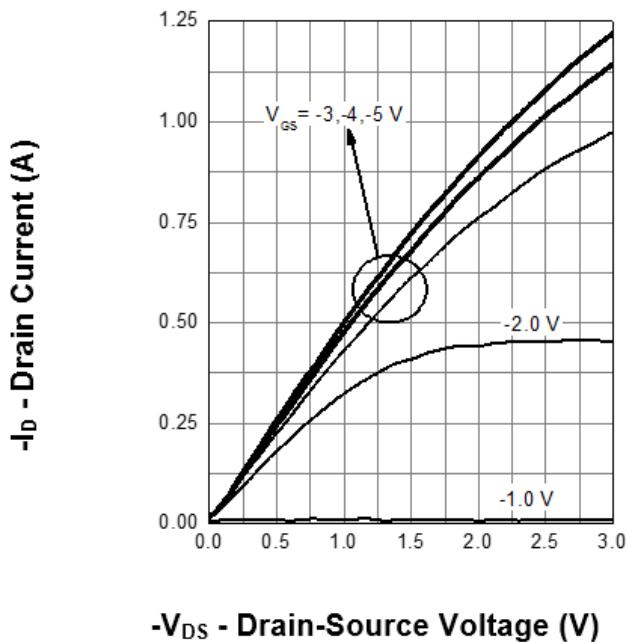


Fig. 1 On-Region Characteristics

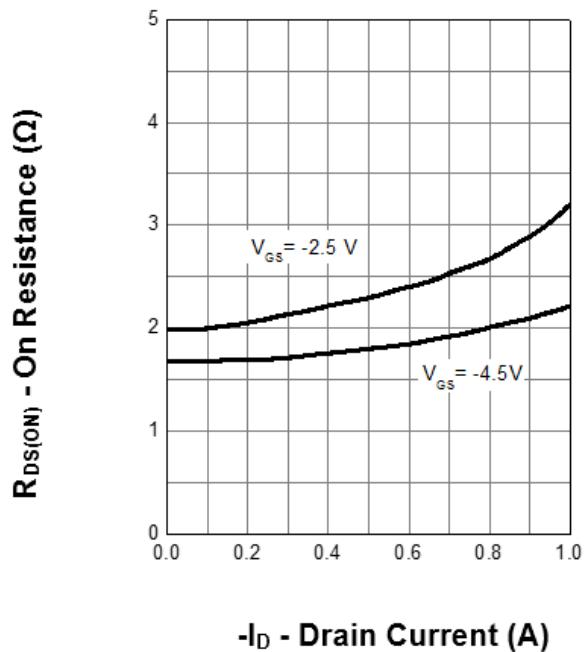


Fig. 2 On-Resistance vs. Drain Current and Gate Voltage

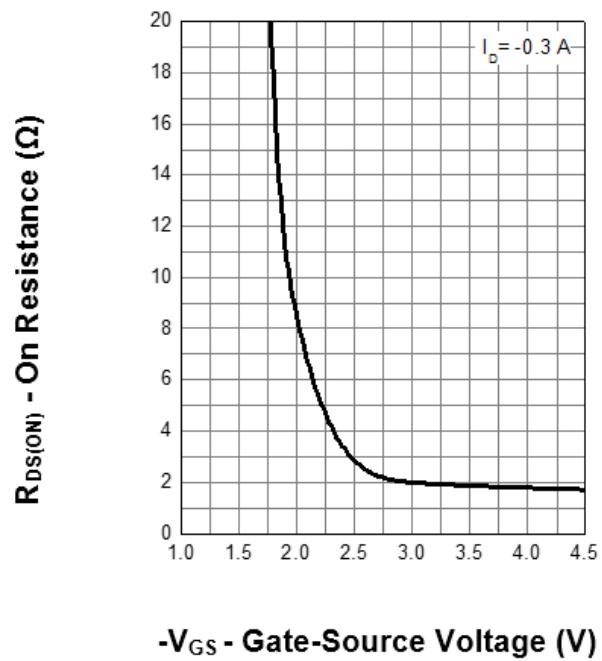


Fig. 3 On-Resistance vs. Gate-Source Voltage

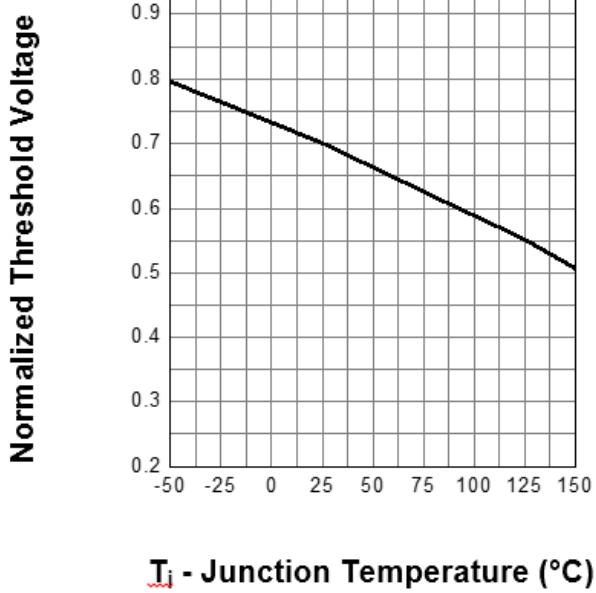


Fig. 4 Gate Voltage vs. Junction Temperature

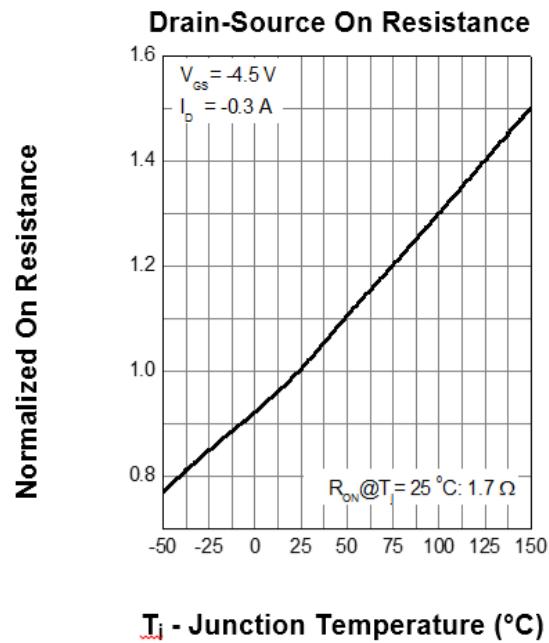
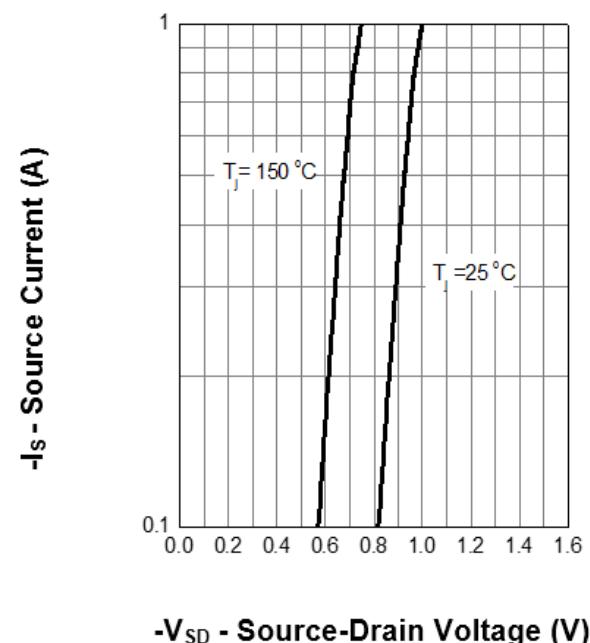
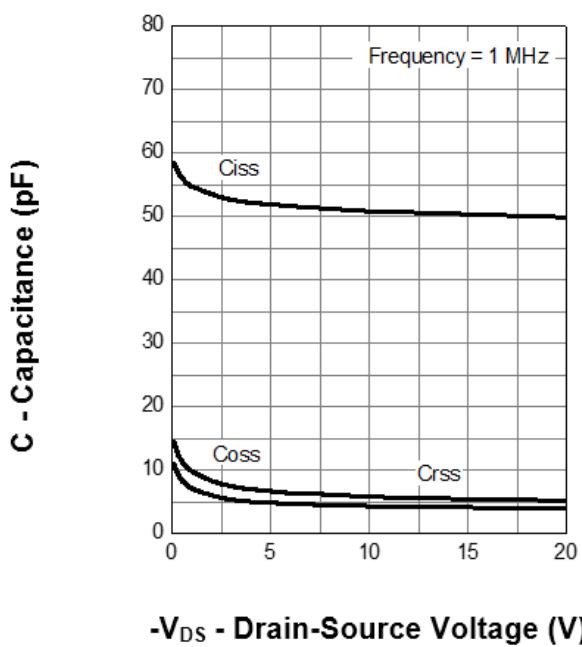


Fig. 5 On-Resistance vs. Junction Temperature

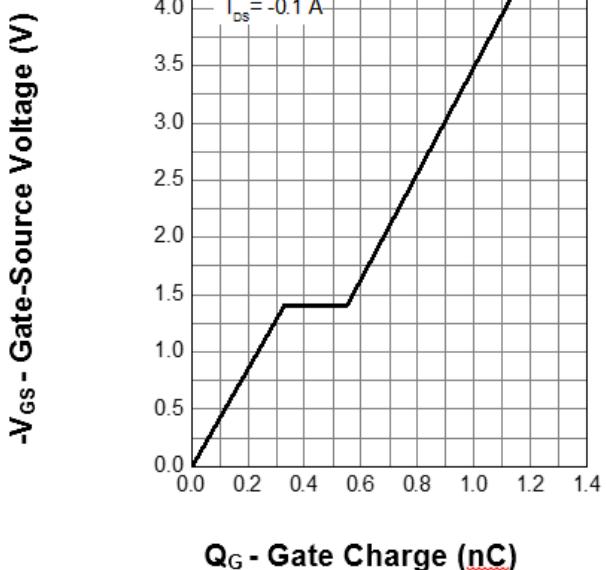


-V_{SD} - Source-Drain Voltage (V)



-V_{DS} - Drain-Source Voltage (V)

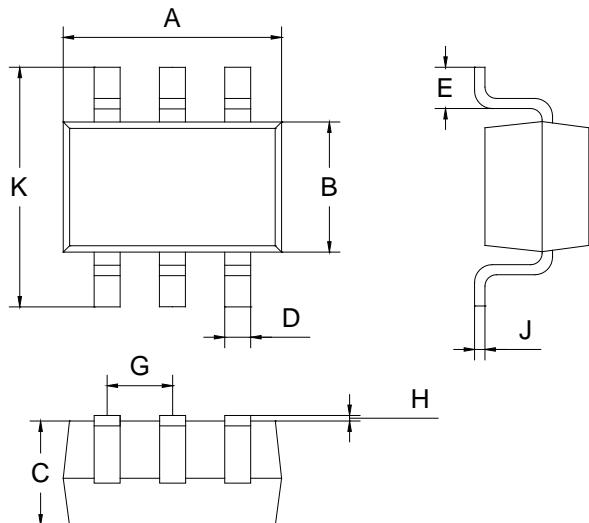
Fig. 7 Capacitance Characteristics



Q_G - Gate Charge (nC)

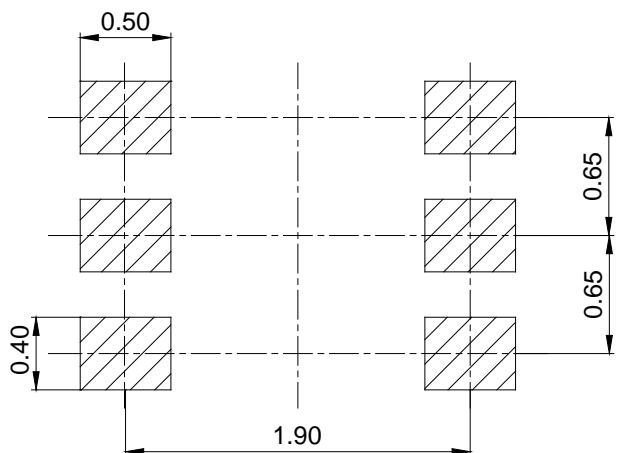
Fig. 8 Gate-Charge Characteristics

Package Outline Dimensions (Unit: mm)



SOT-363		
Dimension	Min.	Max.
A	2.00	2.20
B	1.15	1.35
C	0.85	1.05
D	0.15	0.35
E	0.25	0.40
G	0.60	0.70
H	0.02	0.10
J	0.05	0.15
K	2.20	2.40

Mounting Pad Layout (Unit: mm)

SOT-363


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