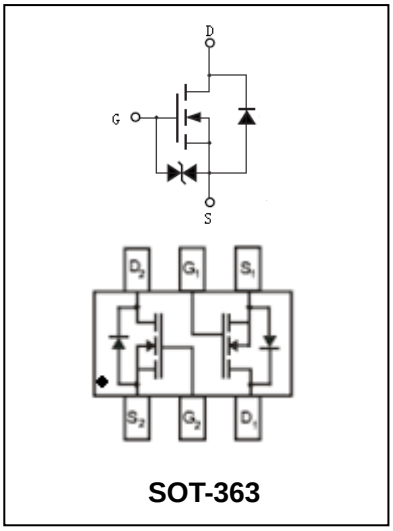
# N-Channel Logic Level Enhancement Mode Field Effect Transistor
# BSS7002DW

## FEATURES

HF

- Low On-Resisrance.
- Low Gate Threshold Voltage.
- Low Input Capacitance.
- Fast Switching Speed.
- Low Input/Output Leakage.




**SOT-363**

## ORDERING INFORMATION

| Type No. | Marking | Package Code |
|---|---|---|
| BSS7002DW | K7D | SOT-363 |

## MAXIMUM RATING @ Ta=25℃ unless otherwise specified

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge voltage Human Body Model | ±2 | kV |
| $V_{DSS}$ | Drain-Source voltage | 60 | V |
| $V_{GSS}$ | Gate -Source voltage | ±20 | V |
| $I_D$ | Drain current -continuous<br>-Pulsed | ±300<br>±800 | mA<br>mA |
| $I_S$ | Source current -continuous<br>-Pulsed | 200<br>0.8 | mA<br>A |
| $P_D$ | Power Dissipation | 200 | mW |
| $R_{\Theta JA}$ | Thermal Resistance,Junction to Ambient | 625 | ℃/W |
| $T_J$, Tstg | Junction and Storage Temperature | -65 to +150 | ℃ |

# N-Channel Logic Level Enhancement Mode Field Effect Transistor
# BSS7002DW

## ELECTRICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

| Parameter | Symbol | Test conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Gate leakage current | $I_{GSS}$ | $V_{GS}$=±20V,$V_{DS}$=0V | | | ±10 | μA |
| Forward voltage | $V_{SD}$ | $I_S$=300mA,$V_{GS}$=0V | | | 1.2 | V |
| Drain-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$=0V,$I_D$=250uA | 63 | | | V |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$ , $I_{DS}$=250uA | 1.1 | | 2.4 | V |
| Drain cutoff Current | $I_{DSS}$ | $V_{DS}$=60V, $V_{GS}$=0V | | | 0.06 | μA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $I_D$=500mA,$V_{GS}$=10V | | | 2.5 | Ω |
| | | $I_D$=50mA,$V_{GS}$=5V | | | 3 | |
| Forward transfer admittance | $\|Y_{fs}\|$ | $V_{DS}$=10V,$I_D$=200mA | 80 | | | mS |
| Input capacitance | $C_{ISS}$ | $V_{DS}$=10V,$V_{GS}$=0V,f=1.0MHz | | | 50 | pF |
| Output capacitance | $C_{OSS}$ | | | | 25 | |
| Reverse transfer capacitance | $C_{RSS}$ | | | | 5 | |
| Turn-On Delay Time | $t_{D(ON)}$ | $V_{DD}$ = 30V, $I_D$= 150mA, $R_L$ = 200Ω, $V_{GS}$= 10V, $R_{GEN}$= 25Ω | | 6 | | ns |
| Rise time | $t_R$ | | | 5 | | ns |
| Turn-Off Delay Time | $t_{D(OFF)}$ | | | 25 | | ns |
| Fall time | $t_F$ | | | 80 | | ns |
| Total gate charge | $Q_g$ | $V_{DD}$=30V,$V_{GS}$=10V $I_D$=200mA | | 3 | 6 | nC |
| Gate-source charge | $Q_{gs}$ | | | 0.6 | | nC |
| Gate-drain charge | $Q_{gd}$ | | | 0.5 | | nC |

# N-Channel Logic Level Enhancement Mode Field Effect Transistor
# BSS7002DW

## TYPICAL CHARACTERISTICS @ Ta=25℃ unless otherwise specified

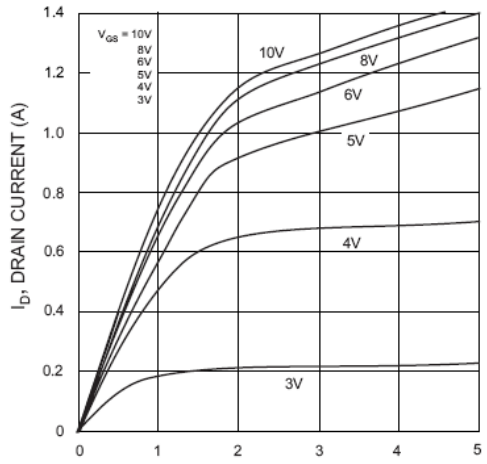



Fig. 1 Typical Output Characteristics

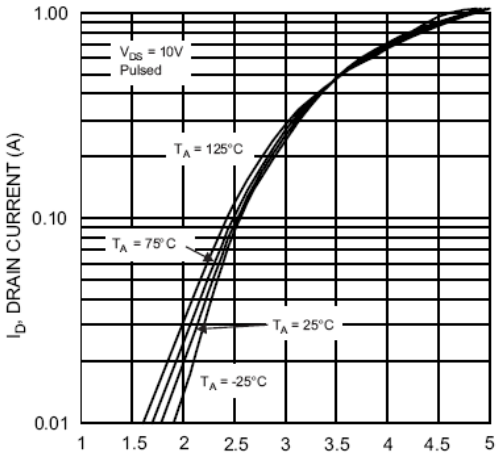



Fig. 2 Typical Transfer Characteristics

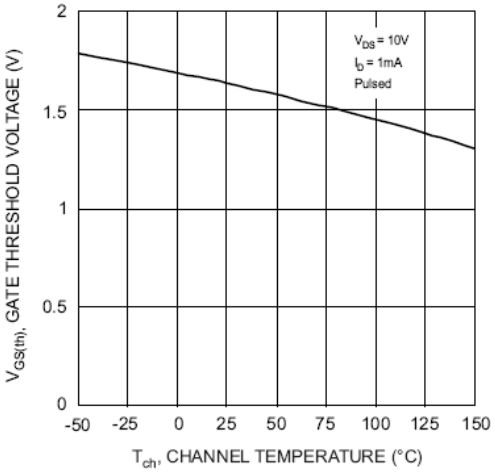



Fig. 3 Gate Threshold Voltage
vs. Channel Temperature

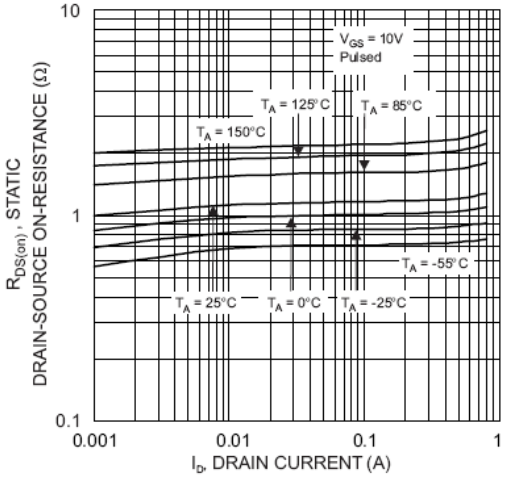



Fig. 4 Static Drain-Source On-Resistance
Vs. Drain Current

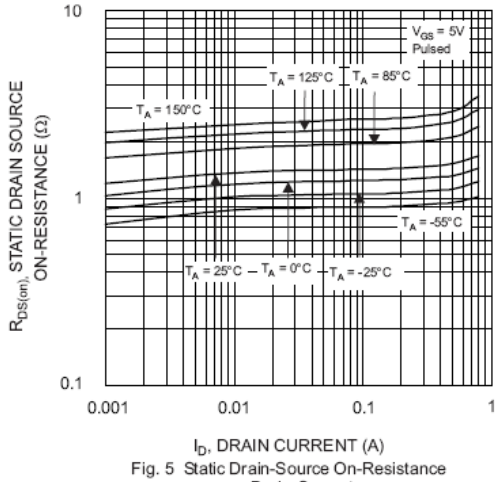



Fig. 5 Static Drain-Source On-Resistance
vs. Drain Current

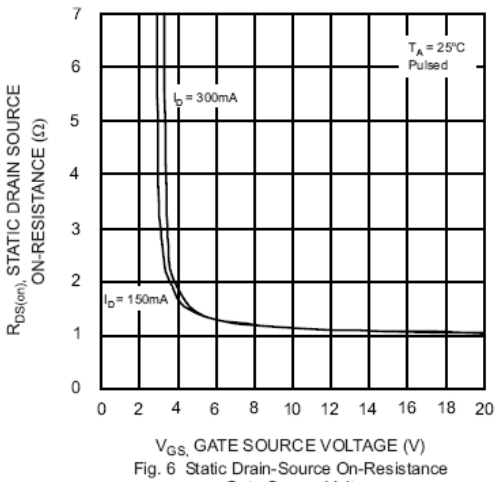
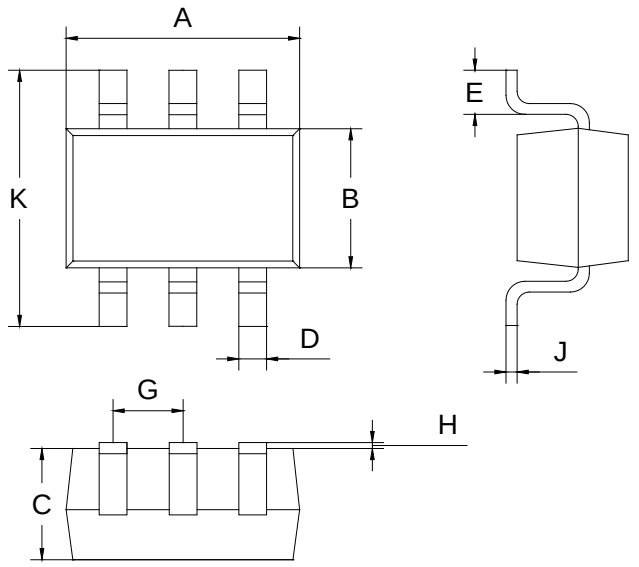



Fig. 6 Static Drain-Source On-Resistance
vs. Gate-Source Voltage

# N-Channel Logic Level Enhancement Mode Field Effect Transistor
# BSS7002DW

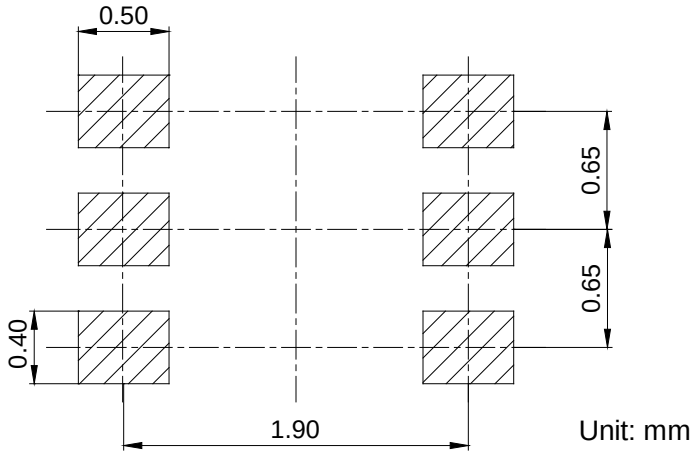
## PACKAGE OUTLINE

Plastic surface mounted package SOT-363




| SOT-363 | | |
|---|---|---|
| Dim | Min | Max |
| A | 2.00 | 2.20 |
| B | 1.15 | 1.35 |
| C | 0.85 | 1.05 |
| D | 0.15 | 0.35 |
| E | 0.25 | 0.40 |
| G | 0.60 | 0.70 |
| H | 0.02 | 0.10 |
| J | 0.05 | 0.15 |
| K | 2.20 | 2.40 |
| All Dimensions in mm | | |

## SOLDERING FOOTPRINT




Unit: mm

## PACKAGE INFORMATION

| Device | Package | Shipping |
|---|---|---|
| BSS7002DW | SOT-363 | 3000/Tape&Reel |