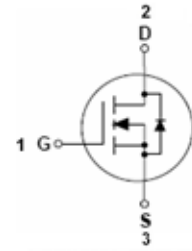


### Features

- Very low FOM  $R_{DS(on)} \times Q_G$
- 100% avalanche tested
- Multi-epi SJ MOSFET
- JESD22-A114-B ESD rating of class 1A per human body model

HF

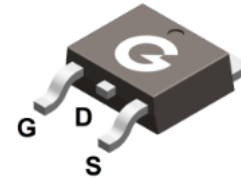


### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

### Mechanical Data

- Case: TO-252
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



TO-252

## Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
SJ80R900D	TO-252	80 pcs / Tube & 2500 pcs / Tape & Reel	SJ80R900D

## Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	800	V
Drain-to-Source Voltage @ $T_J(\text{Max.})$	$V_{DSS}$	850	V
Gate-to-Source Voltage	$V_{GSS}$	$\pm 30$	V
Continuous Drain Current ( $T_C = 25^\circ\text{C}$ )	$I_D$	6	A
Continuous Drain Current ( $T_C = 100^\circ\text{C}$ )		3.6	A
Pulsed Drain Current ( $t_p = 10\mu\text{s}$ , $T_C = 25^\circ\text{C}$ )	$I_{DM}$	18	A
Single Pulse Avalanche Energy <sup>*3</sup>	$E_{AS}$	62	mJ

## Thermal Characteristics

Parameter	Symbol	Value	Unit
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	63	W
Thermal Resistance Junction-to-Ambient <sup>*1</sup>	$R_{\theta JA}$	25	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	2	$^\circ\text{C/W}$
Operating Junction Temperature Range	$T_J$	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

### Electrical Characteristics (@ $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
$V_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	800	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	-	1	$\mu A$
		$V_{DS} = 800V, V_{GS} = 0V, T_J = 150^\circ\text{C}$	-	-	100	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 30V, V_{DS} = 0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$R_{DS(ON)}$	Static Drain-Source On-resistance <sup>*2</sup>	$V_{GS} = 10V, I_D = 3A$	-	0.85	0.95	$\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5	3.4	4.5	V
$R_G$	Gate Resistance	$V_{GS} = 0V, f = 1\text{MHz}$	-	13	-	$\Omega$
<b>Dynamic Characteristics</b>						
$C_{ISS}$	Input Capacitance	$V_{GS} = 0V$	-	528.6	-	pF
$C_{OSS}$	Output Capacitance	$V_{DS} = 100V$	-	16	-	
$C_{RSS}$	Reverse Transfer Capacitance	$f = 1.0\text{MHz}$	-	0.31	-	
<b>Switching Characteristics</b>						
$t_{d(ON)}$	Turn-on Delay Time <sup>*4</sup>	$V_{DD} = 400V$ $R_G = 25\Omega$ $I_D = 6A$	-	41	-	ns
$t_r$	Turn-on Rise Time <sup>*4</sup>		-	11	-	
$t_{d(OFF)}$	Turn-Off Delay Time <sup>*4</sup>		-	75	-	
$t_f$	Turn-Off Fall Time <sup>*4</sup>		-	37	-	
$Q_G$	Total Gate-Charge	$V_{DD} = 640V$	-	14.1	-	nC
$Q_{GS}$	Gate to Source Charge	$V_{GS} = 10V$	-	3.05	-	
$Q_{GD}$	Gate to Drain (Miller) Charge	$I_D = 6A$	-	7.06	-	
<b>Source-Drain Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage <sup>*2</sup>	$I_{SD} = 3A, V_{GS} = 0V, T_J = 25^\circ\text{C}$	-	0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 6A, V_R = 400V$ $di/dt = 100A/\mu s$	-	345	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	2.5	-	$\mu C$
$I_{rrm}$	Peak Reverse Recovery Current		-	16.7	-	A

Notes:

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper
- The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- The  $E_{AS}$  data shows Max. rating. The test condition is  $V_{DD} = 50V, V_{GS} = 15V, L = 10mH$
- Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@  $T_J = 25^\circ\text{C}$  unless otherwise specified)

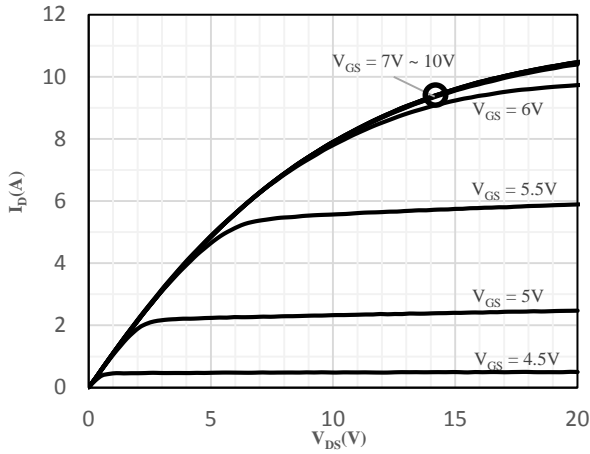


Fig 1 Typical Output Characteristics

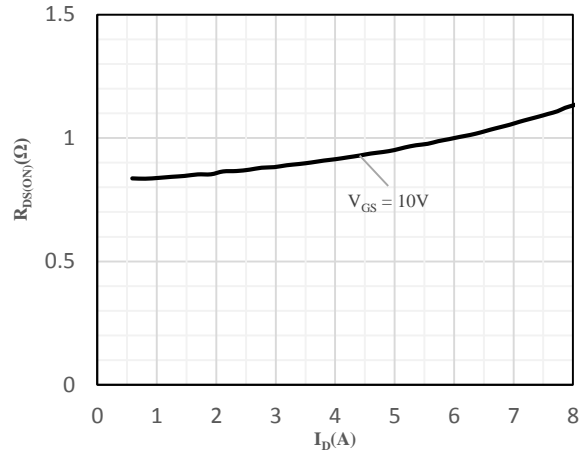


Fig 2 On-Resistance vs. Drain Current and Gate Voltage

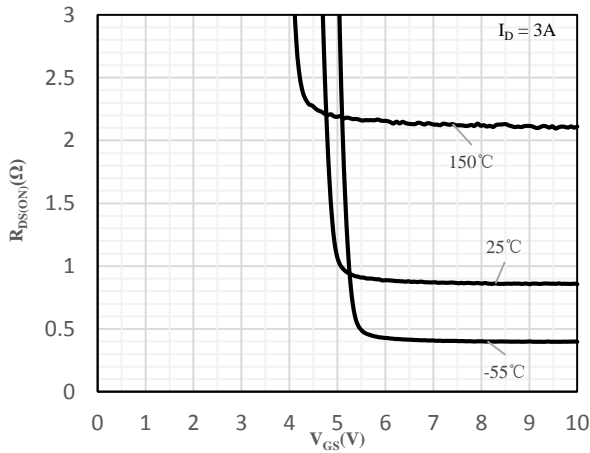


Fig 3 On-Resistance vs. Gate-Source Voltage

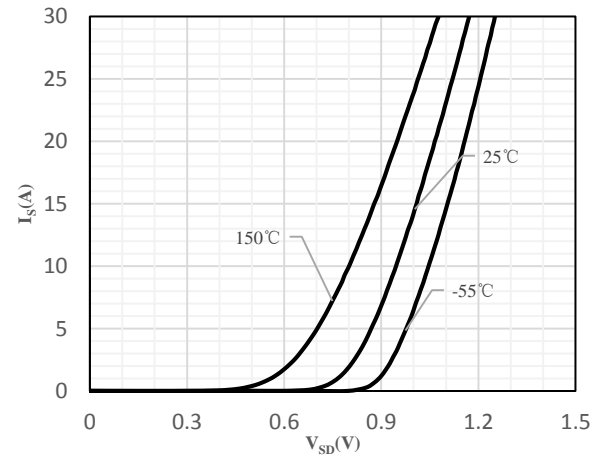


Fig 4 Body-Diode Characteristics

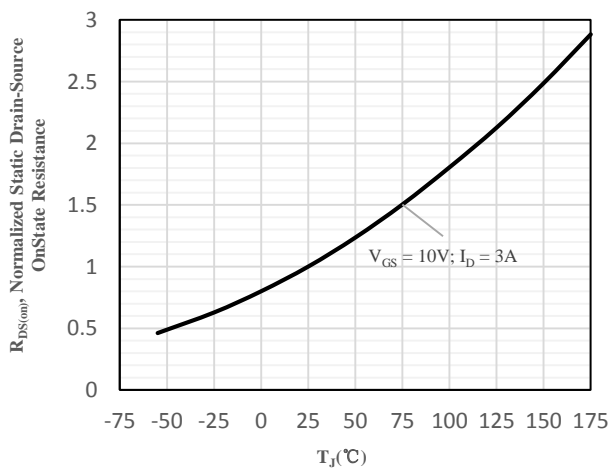


Fig 5 Normalized On-Resistance vs. Junction Temperature

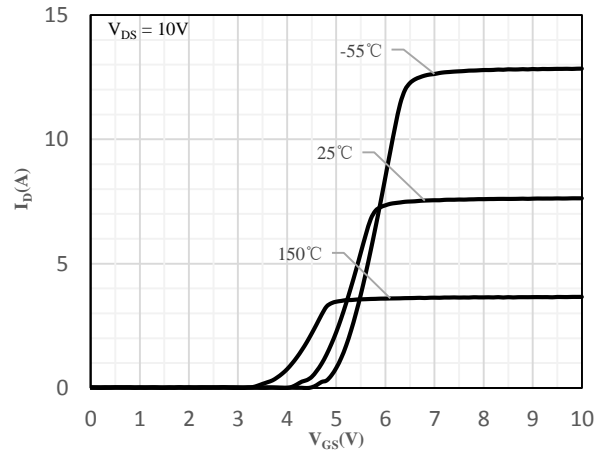


Fig 6 Transfer Characteristics

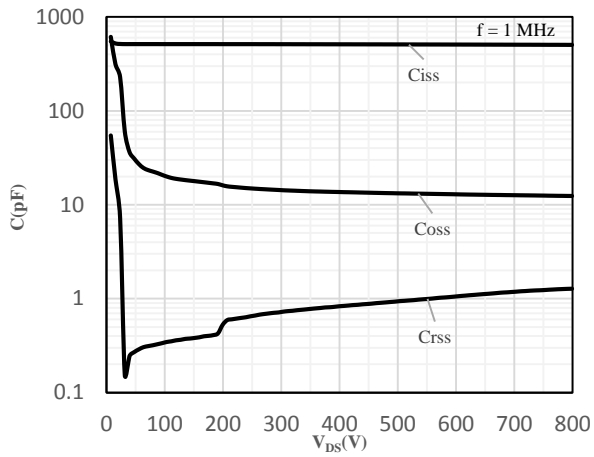


Fig 7 Capacitance Characteristics

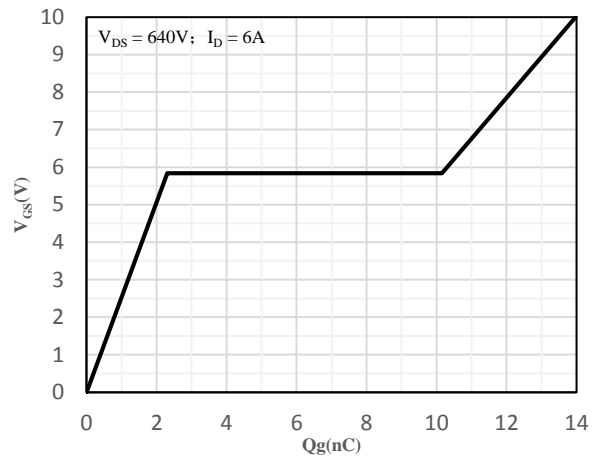


Fig 8 Gate-Charge Characteristics

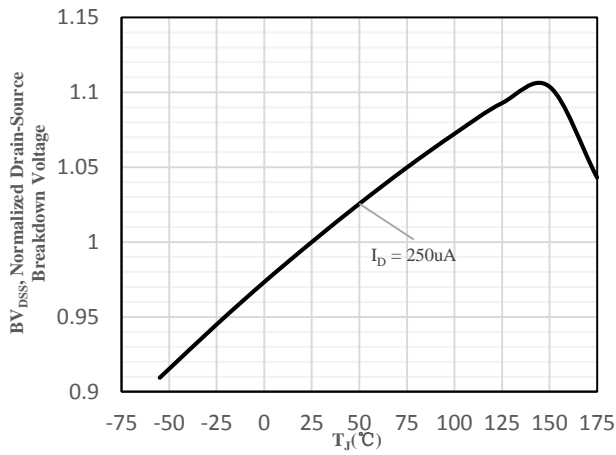


Fig 9 Normalized Breakdown Voltage vs. Junction Temperature

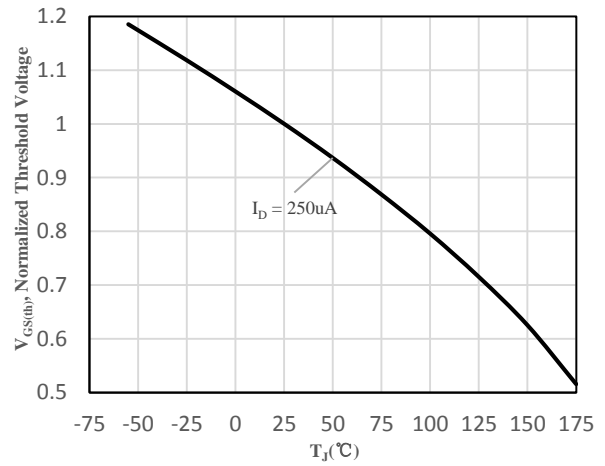


Fig 10 Normalized  $V_{GS(th)}$  vs. Junction Temperature

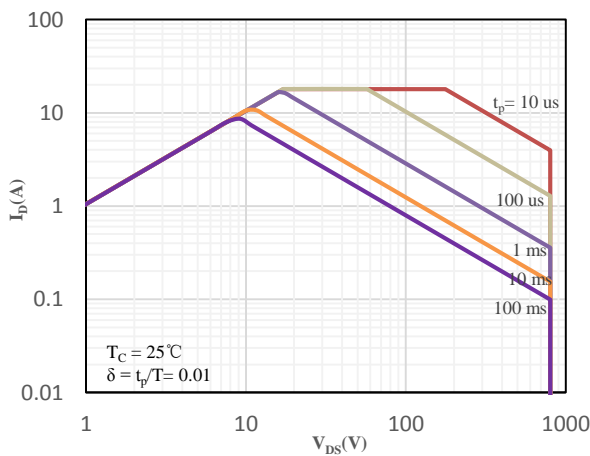


Fig 11 Safe Operation Area

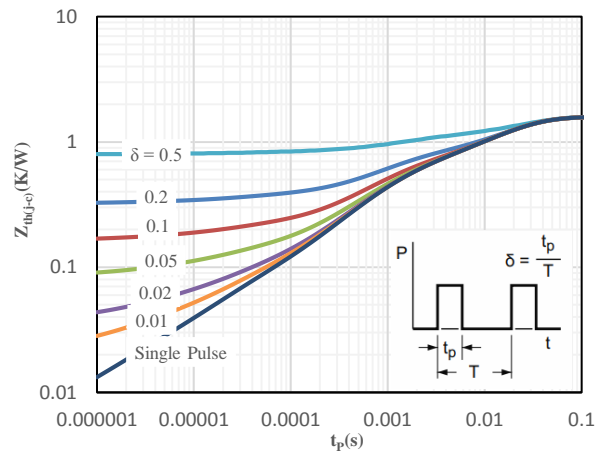
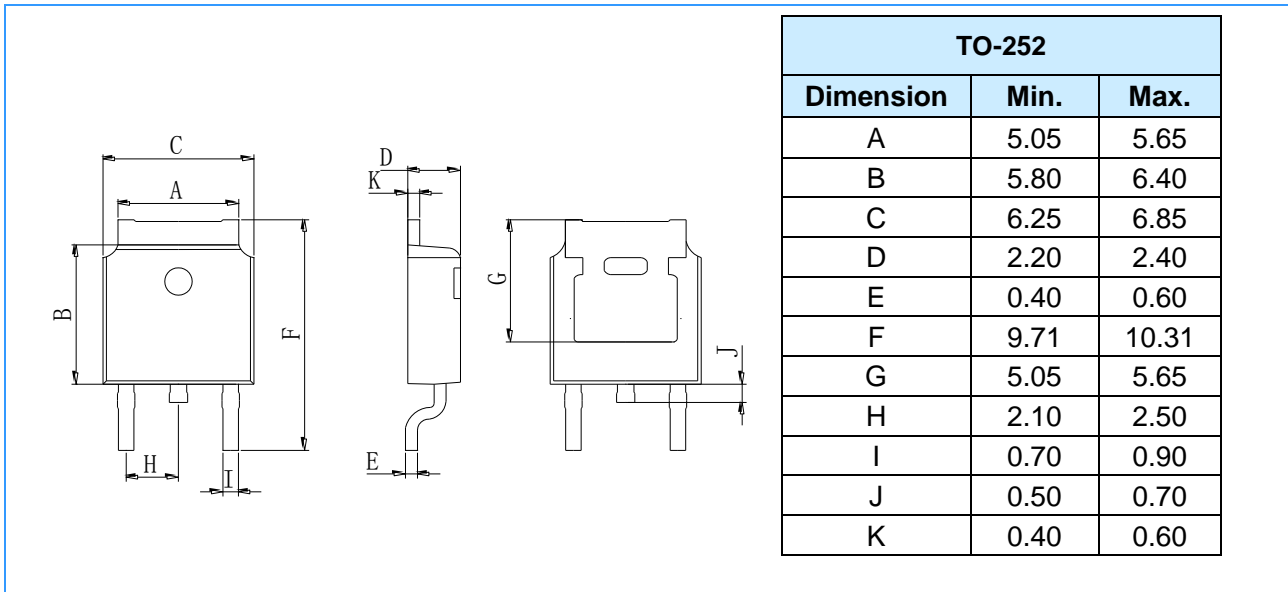
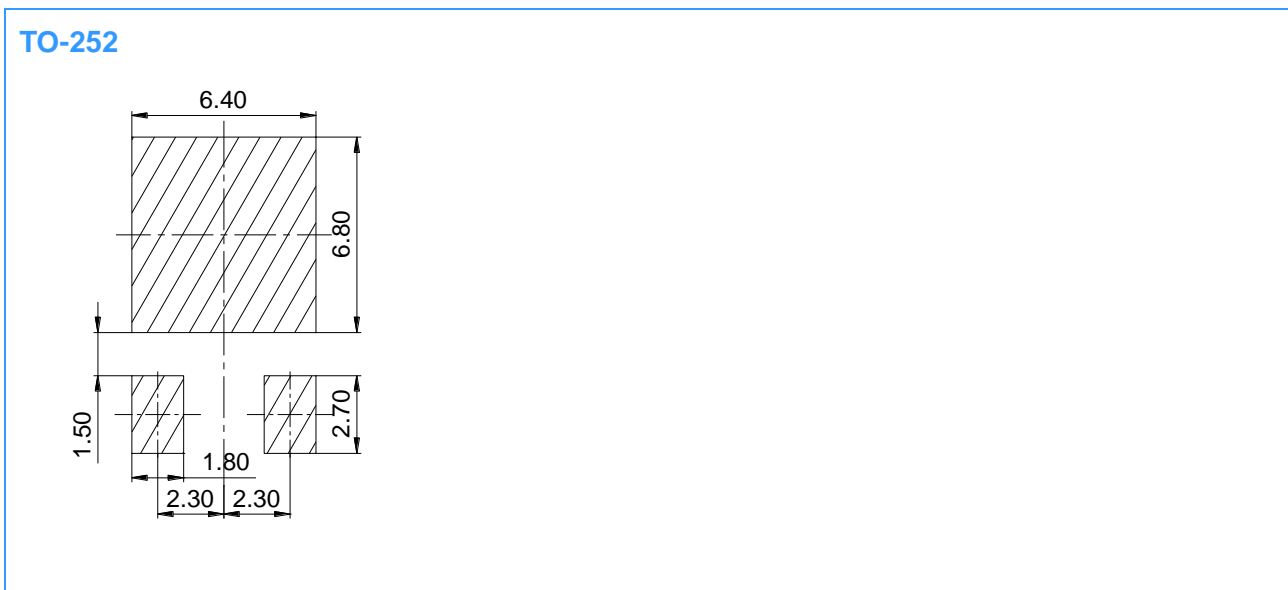


Fig 12 Maximum transient thermal impedance

**Package Outline Dimensions** (Unit: mm)



**Mounting Pad Layout** (Unit: mm)



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